AMENDMENTS TO THE SPECIFICATION

Please replace paragraph **[003]** on page 1 with the following amended **[003]** paragraph.

[0003] As shown in Fig. ~~9~~ 22 of the present application, this memory is composed of a gate electrode 909 formed on a P type well region 901 through a gate insulating film, and a first N type diffusion layer region 902 and a second N type diffusion layer region 903 formed on the surface of the P type well region 901. The gate insulating film is composed of so-called ONO (Oxide Nitride Oxide) film in which a silicon nitride film 906 is interposed between silicon oxide films 904 and 905. In the silicon nitride film 906, there are formed memory holing portions 907, 908 in the vicinity of the edge portions of the first and second N type diffusion layer regions 902, 903.